IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-9 (Canceled)

10. (Currently Amended) An ATM (Asynchronous Transfer Mode) PON (Passive Optical Network) ONU (Optical Network Unit) controlling apparatus, comprising:

a cell receiving means for receiving an ATM cell from the PON downstream data and transferring the ATM cell through a receiving UTOPIA interfacing means to an external ~~means~~ device and transferring a message in a PLOAM (Physical Layer Operation and Maintenance) cell to a message processing means by demultiplexing;

a cell transmitting means for transmitting the ATM cell received through a transmitting UTOPIA interfacing means in a granted slot and transferring in upstream by loading the message being on standby in payload of the PLOAM cell when the PLOAM cell is transmitted; and

the message processing means for setting internal signals by processing the received message or instructing operation of a plurality of functional blocks, and transferring the message requested by the plurality of functional blocks through the cell transmitting means;

wherein an external transceiver generates from received bit stream a recovered byte clock and associates received byte stream by blindly gathering every 8 bits to byte for downstream data regardless of correct byte boundaries, and a following byte delineation logic selects correct byte stream out of 8 possible bits shifted byte streams by monitoring a cell delineation result;

wherein the cell receiving means generates a pulse which indicates a start of a frame reference, and the pulse is delayed before setting a start point of counters governing an upstream frame timing, thus implementing desired amount of a relative phase difference between downstream frames and upstream frames;

wherein an initial pulse delay is done for an initial delay amount before conducting ranging, but after ranging, an amount of time delay received from an optical line termination (OLT) is added to the delay amount so that a round trip time for the ONU becomes equal to a pre-defined round trip time used for all ONUs; and

wherein the amount of the pulse delay also reflects the difference of from 0 to 7 bits between the recovered byte clock and the selected correct byte stream phase, and of total delay which is in unit of bits, the amount which can be delayed in byte processing with byte clock is applied in byte processing logic and a remaining bit delay of from 0 to 7 bits is applied in the cell transmitting means by shifting the data bit-wise, and also the remaining bit delay information is outputted from the chip so that the laser enable signal can also be equivalently delayed with external bit processing logic to thereby remove the uncertainty of measured RTT value arising from the blindness of the byte clock recovery after power-up and makes the RTT value to appear to be the same every time the ONU system is powered up or byte clock is newly recovered with different random phase with respect to the correct byte boundaries.

11. (Previously Presented) The apparatus as recited in claim 10, wherein the cell transmitting means outputs an enable signal for minislot payload and receives mini-slot payload bytes and sends them upstream on the minislot for using an arbitrary mini-slot report format.

12. (Previously Presented) The apparatus as recited in claim 10, wherein the cell receiving means includes:

a cell and byte delineating means for receiving a byte stream from an external serial/parallel transformer and delineating the cell and the byte;

a descrambling means for receiving a scrambled cell stream from the cell and byte delineating means and descrambling data with synchronization to the received data;

a BIP (Bit Interleaved Parity) comparing means for computing a BIP value for the data received from the descrambling means for a predetermined period and comparing the computed BIP value with the received BIP value;

a frame synchronizing means for synchronizing the frame by finding a location of the PLOAM cell and a frame starting point for the data received from the descrambling means;

a receiving demultiplexing means for demultiplexing the ATM cell, the PLOAM cell, and a grant value and a message received thereto from the data transferred from the frame synchronizing means;

a look-up processing means for reading the table depending on a VPI (Virtual Path Identifier) by using the ATM cell transferred from the receiving demultiplexing means to check whether it is to be received or dechurned;

a receiving UTOPIA interfacing means for storing the ATM cell transferred from the look-up processing means and transferring the stored ATM cell in response to an external request;

a grant decoding means for decoding the grant value received from the receiving demultiplexing means; and

a grant table for receiving and storing a writing signal from the grant decoding means.

13. (Previously Presented) The apparatus as recited in claim 12, wherein the cell receiving means further includes:

a header error inspecting means for inspecting header error for the ATM cell transferred from the receiving demultiplexing means to correct the error or to abandon the cell;

a dechurning means for receiving ATM related information from the look-up processing means and, if necessary, dechurning the payload of the received ATM and changing a churning key;

a memory arbitrating and interfacing means for arbitrating connection table reading and writing requests from the message receiving processing means processing the received message from external and a CPU (Central Processing Unit) interface to process reading and writing, the content of the data written to or read from the memory being information on whether, for the given VPI value, to pass the received ATM cell to the receiving UTOPIA processing and whether to dechrun the received ATM cell; and

a dual-port memory for storing information for VPI receiving and dechurning by using the VPI as an address.

14. (Previously Presented) The apparatus as recited in claim 10, wherein the cell transmitting means includes:

a transmitting UTOPIA interfacing means for storing the ATM cell depending on an external request and transferring the ATM cell;

a transmitting multiplexing means for determining category of the cell transferred via a grant table by the frame count and the slot counter of internal, transmitting an enable signal to a transmitting message processing means, a mini-cell generating means or the transmitting UTOPIA interfacing means, and generating slot data including transmitting overhead by multiplexing resultant data coming according to the enable signals;

a BIP inserting means for computing a BIP value for all data except for the overhead and the mini-cell for data transferred from the transmitting multiplexing means as instructed by the transmitting multiplexing means and inserting the BIP value into last byte of the PLOAM cell;

a scrambling means for scrambling all data except for the overhead as instructed by the transmitting multiplexing means or the BIP inserting means; and

a ranging counting means for delaying the synchronization pulse coming from the receiver frame synchronizing means as many clocks as set by the delay Td which is delivered in the received message.

15. (Previously Presented) The apparatus as recited in claim 14, wherein the cell transmitting means further includes:

a mini-cell generating means for generating payload of the mini-cell by using buffer information of the transmitting UTOPIA interfacing means or data from the external interface; and

a bit delaying means for selectively delaying the transmitted data transferred through the scrambling means using the value transferred from the ranging counting means.

16. (Previously Presented) The apparatus as recited in claim 10, wherein the message processing means includes:

a CRC (Cyclic Redundancy Check) checking means for checking the CRC for the message transferred from the receiving demultiplexing means to transfer the message;

a receiving message processing means for decoding the message transferred from the receiving demultiplexing means, setting each register depending on the message, and triggering other functional blocks;

a transmitting message processing means for receiving a message insertion instruction from the transmitting multiplexing means and generating a predetermined message depending on a message transmitting request from various blocks;

a ranging state machine for ranging by managing operation;

a timer for finding out a time out required for ranging; and

a CPU interfacing means for reading a message transferred via the memory arbitrating and interfacing means in a format that can be read by the CPU.

17. (Previously Presented) The apparatus as recited in claim 16, the message processing means further includes:

a receiving message storing means for receiving and storing a message, to be processed by a software, from the receiving message processing means and interrupting a CPU interfacing means with the number of the messages for the CPU to read the messages;

a churning key generating means for generating a new churning key depending on an instruction from the receiving message processing means to transfer the key to the dechurning means and requesting the new churning key message transmitting to the transmitting message processing means;

a BIP error accumulating means for accumulating the number of the BIP errors transferred from the BIP comparing means to notify it to the CPU interfacing means and transferring the accumulated error value to the transmitting message processing means periodically;

a transmitting message storing means for receiving a message from the CPU interfacing means to transfer it to the transmitting message processing means;

a response message processing means for receiving an acknowledge message from the receiving message processing means to transfer it to the transmitting message processing means; and

a serial number receiving means for receiving a serial number of a corresponding ONU from a register set by the CPU interfacing means or an external interface.